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EV182661221 *Julen*

UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/875,501
Filing Date June 4, 2001
Inventor Klaus Florian Schuegraf et al.
Assignee Micron Technology, Inc.
Group Art Unit 2815
Examiner E. Ortiz
Attorney's Docket No. MI22-1741
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects,
and Wordline, Transistor Gate, and Conductive Interconnect Structures

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to
the United States patents and other references listed on the attached Form PTO-1449.

No admission is made regarding whether all the submitted references are prior art.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 12-27-02

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/332,271
 Priority Filing Date June 11, 1999
 Inventor Klaus Florian Schuegraf et al.
 Assignee Micron Technology, Inc.
 Priority Group Art Unit 2815
 Priority Examiner E. Lee
 Attorney's Docket No. MI22-1741
 Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects,
 and Wordline, Transistor Gate, and Conductive Interconnect Structures



INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449


The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional of co-pending Application Serial No. 09/332,271, filed on June 11, 1999. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 6-4-01

Attorney: 
 D. Brent Kenady
 Reg. No. 40,045

EL4 780540

Sheet 1 of 1

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
MI22-1741SERIAL NO.
Filed HerewithLIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)APPLICANT
Klaus Florian Schuegraf et al.FILING DATE
Filed HerewithGROUP
Unknown

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
EO	AA	5,425,392	06/95	Thakur et al.			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AL							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

EO	AK		Taishi Kubota et al.; "The Effect of the Floating Gate/Tunnel SiO ₂ Interface on FLASH Memory Data Retention Reliability"; 1994; 2 pages
EO	AL		Shoue Jen Wang et al.; "Effects of Poly Depletion on the Estimate of Thin Dielectric Lifetime"; IEEE Electron Device Letters, Vol. 12, No. 11, November 1991; pp. 617-619
EO	AM		Klaus F. Schuegraf et al.; "Impact of Polysilicon Depletion in Thin Oxide MOS Technology"; 1993; pp. 86-88
EO	AN		E. H. Snow et al.; "Polarization Phenomena and Other Properties of Phosphosilicate Glass Films on Silicon"; Journal of the Electrochemical Society, March 1966; pp. 263-269

EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.